ASIC for Monitoring of Human Motion

H. Takao, K. Maenaka, K. Higuchi, O. Nizhnik, O. Vinluan, U. Maksudi, T. Bartley

***Abstract*— In this paper, a novel ASIC for monitoring of human motion developed in the "JST-ERATO Maenaka Sensing Fusion Project" is presented. This LSI includes both analog components for various kinds of interface for sensors and digital components for digital processing and information control with micro-processor. T8051-compatible core is integrated with peripherals and program/data memories on a single chip. The ASIC is designed to realize very low power consumption below 100μW in average for a longer battery life of the sensing system.**

I. Introduction

Fusion sensing is very promising approach for monitoring of human motion. In the "JST-ERATO Maenaka Sensing Fusion Project", sensors integrated in the system for human motion monitoring are accelerometer, humidity sensor [1], light sensor, pressure sensor [2], temperature sensor, and ECG detector. So, interface and data processing of the sensor signals are required functions for the ASIC of system. Also, low power consumption is an important performance of the ASIC chip. Since a longer battery life is advantageous to monitor a human's motion for a long time, average power consumption below 100μW is required in the state-of-the-art technology in the field. The ASIC in the project has been developed to satisfy the above requirements.

II. System Configuration of the ASIC

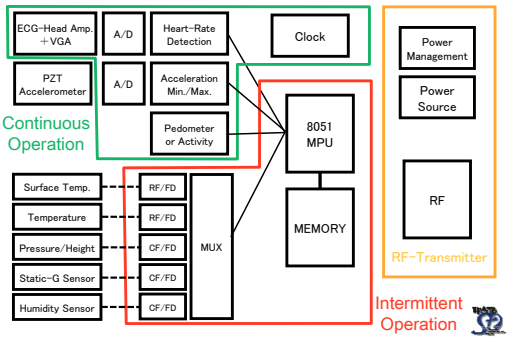

Fig. 1 System block diagram of the ASIC for monitoring of human motion.

Fig. 1 shows the system configuration diagram of the ASIC developed in the project for human monitoring. It integrates analog interface circuit for the sensors. The sensors are micro-devices and fabricated by MEMS technology. Since the signal outputs of some sensors are obtained as resistance change or capacitance change, they are translated into digital signal at the front-end. Signal of resistive sensors is converted with combination of resistor-to-frequency convertor and frequency-to-digital converter (RF/FD), while signal of capacitive sensors is converted with combination of capacitor-to-frequency converter and frequency-to-digital converter (CF/FD) in the figure. Voltage signals of ECG and PZT accelerometer is amplified and converted to digital signal with ADC. They are utilized for digital processing of heart-rate detection, detection of Max/Min acceleration, and pedometer for activity monitoring.

The digital core of 8051 microprocessor, and program/data memory block are integrated around the digital core as peripherals. The blocks enclosed in red line works in intermittent operation mode to reduce the effective (average) power consumption. The estimated power consumption of the blocks is below 5μW. On the other hand, the blocks enclosed in the green line operate in continuous mode. Although the power consumption of the blocks reaches 33μW, the total power consumption of the overall system including RF-transmitter will be below 100μW. This is low enough to realize required battery life, and better than the performances of existing systems in the present fusion sensing field.

III. Developed Examples of Very Low-Power Blocks

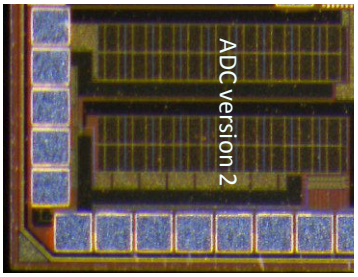

Fig. 2 Developed very low power 8-bit SAR-ADC block.

A very low power circuit blocks have been developed in the ASIC. Fig. 2 shows an example of very low power circuit block (SAR-ADC). Limiting the signal bandwidth at the lowest bandwidth for conversion, 1.53μW power consumption of ADC has been achieved for our purpose.

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References

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