Energy-Efficient, 0.1 nJ/conversion Temperature Sensor with Time-to-Digital Converter and 1 °C Accuracy in -6 to 64 °C Range

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***Abstract*—The proposed time-to-digital converter based on a Schmitt trigger monostable multivibrator and an external thermistor with a negative temperature coefficient is used to implement an ultra-low-power (105 pJ/conversion measured) temperature sensor. It has significantly lower power (1/250) compared to state of the art diode/ADC temperature sensors. The proposed temperature sensor also dissipates 1/3 of the power of state of the art frequency-to-digital converter (ring oscillator) based temperature sensors. Furthermore, the proposed circuit is nearly immune to process and power supply variation thanks to the ratiometric nature of the Schmitt trigger threshold levels. An on-chip MIM capacitor and external thermistor are the precision analog components used to set the gain of the sensor. All other circuitry in the proposed temperature sensor is digital, and the output is the measured temperature in a 2's complement, 8-bit digital code with the LSB representing 0.5 °C.**

I. INTRODUCTION

Monitoring human activity for health hazards is an application in high demand [1]. Currently, state of the art temperature sensors are mostly based on a proportional to absolute temperature (PTAT) diode voltage source [2]. But temperature-monitoring systems are very limited in terms of longevity and autonomy because of limited battery life. Modern wireless sensor nodes are evolving to operational power below 100 uW, with digital cores operating below 1 V power supply voltage. Diode-based sensors are limited to power supply voltages above 1.4 V [2] because the output reference voltage is fixed to 1.25 V (the bandgap of silicon at absolute zero). Attempts to circumvent this limitation by means of a current-mode bandgap reference [3] were not generally successful because the current-mode reference which means to replace PTAT voltage output is susceptible to process variation (PV), resulting in state of the art gain error of 1 % if untrimmed [3]. Furthermore, the PTAT source-based temperature sensor is difficult to operate at low duty cycle because the low-power operational amplifier included typically has a long startup time. The startup time of the op-amp is difficult to minimize because of the tradeoff between op-amp slew rate and startup time. Furthermore, the op-amp power dissipation has a practical lower limit imposed by the large RC-network required in the frequency correction loop. The ADC may also be power bottleneck. Although modern successive approximation register (SAR) ADCs have reached the impressive 15 fJ/step levels of power efficiency [4], the power dissipation of the reference voltage source needed by all ADCs to set the ADC gain would dominate the sensor power dissipation. Ratiometric ADCs (using power supply as voltage reference) are possible but generally incompatible with PTAT source-based temperature sensors. For these reasons, diode-based temperature sensors are power-hungry components with power dissipation of a few microwatts, potentially dominating the power dissipated by low-power wireless sensor nodes. The estimated lower energy limit of PTAT source-based temperature sensor (10 nJ/sample) is close to the current state of the art (27 nJ/sample) [2].

An alternative considered by designers is the frequency-to-digital converter (FDC). FDCs employ a reference quartz oscillator and a temperature-controlled ring oscillator [5]. But because the ring oscillator frequency is a function not only of temperature, but of power supply voltage as well, FDC-based sensors need a precise voltage regulator as well. At low power supply voltage and power dissipation, such regulators become increasingly susceptible to electromagnetic interference, especially switching noise. Even small amounts of charge (a few fC), coupled to a regulated voltage source with µW-level driving strength, may induce an offset in the measured temperature. Furthermore, additional linear regulators in the sensing system increase the power dissipation because of the regulator voltage drop and built-in op-amp power dissipation. Also, in the case of duty-cycle operation of the FDC, some power is either bled to maintain stability of voltage regulator while the FDC is shut down, or spent to power-up the voltage regulator (if voltage regulator is used in the same duty-cycle operation). Because the voltage regulator normally includes a reference voltage generator and op-amp, voltage-regulated FDC-based temperature sensors typically have similar power

dissipation constraints as PTAT source-based temperature sensors.

Also, special attention is necessary for the temperature signal transfer to MCU (microcontroller unit). For example, consider the estimated power dissipation of most common architectures of data transmission – serial and parallel (Table 1). Sensor I2C slave leakage power is estimated to be 200 nW, but can be reduced ~25 times by selecting an ultra-low-leakage CMOS process. The estimation for MCU I2C port leakage assumes the port is shared by X sensors, and the MCU is a 3 pJ/cycle T8051 MCU operating at 1.0 V power supply.

TABLE I. COMPARISON OF POWER DISSIPATION FOR INTER-CHIP DATA TRANSMISSION

I2C-based interface (4.7 kΩ Pull-up, 34 kbit/s, 1 sample/s)	
Component	***Power, nW***
Sensor I2C slave leakage power	200
I2C transfer, 24 bits	150
MCU I2C port leakage	<Y
MCU operation to transmit/receive 24 bits	2
Total	352
Parallel port-based interface (8 bits)	
Sensor port leakage power	8
Data transfer (9 bits – including request line)	0.1
MCU port leakage power	25
MCU operation to request/receive 8 bits	0.3
Total	33.4

Significant additional power loss may happen if the signal received by MCU needs data processing, as is common for FDC-based temperature sensors. Calibration, scaling, table lookup, and calculation of the logarithm all spend energy. Dependent on the processing, these losses can be 1-100 /sample with the microcontroller technology of 2013. Table I shows that the power dissipation of the sensor system based on parallel port communication is approximately 1/10 of serial-port-based system. Although parallel-port interfaces have issues with scalability (it is impractical to put more than 8 parallel ports on a single MCU), this is not of concern for ultra-low power sensor nodes, typically possessing only 2 or 3 sensors.

II. TEMPERATURE SENSOR ARCHITECTURE

A. Architectural Description

According to discussion in Section I, the best low-power temperature sensors must have the following features:

- Do not require precision reference voltage
- High power supply rejection ratio (PSRR)
- Insensitive to PV
- Capable of low duty-cycle operation (no op-amps)
- Calibrate and format the data
- Produce digital output in parallel format

A temperature sensor conforming to the above list must employ the strengths of digital circuitry: good PSRR and insensitivity to PV. Therefore, some sort of time-to-digital converter (TDC) or frequency-to-digital converter (FDC) as opposed to analog-digital converter (ADC) is necessary.

Because each change of voltage on internal nodes will require spending additional power for node capacitance recharging, the TDC operation is strongly favored over FDC operation mode for an ultra-low-power sensor. The ideal TDC would swing the voltage over the RC chain with temperature-dependent time constant only once. Multiple swings used with averaging of the measured RC time-constant may yield improved S/N ratio of the sensor output, but are not justified if sensor is not noise-limited.

Measurement of the RC time-constant requires a comparator between the digital and analog domains with 2 exactly ratiometric (proportional to power supply voltage) thresholds to facilitate a good PSRR. The simplest such circuit (6-transistors Schmitt trigger [6]) has the simulated performance (in the UMC 0.11um eFlash process) shown in Table II.

TABLE II. SIMULATED SCHMITT TRIGGER PARAMETERS

Parameter	***Value***
Transistor length (all transistors)	110 nm
Transistor width (all transistors)	270 nm[a]
Power supply voltage range tested	0.7 V – 4 V
Worst case PSRR, falling input voltage	50 dB (0.003 %/%)
Worst case PSRR, rising input voltage	47 dB (0.004 %/%)
Lower threshold voltage	0.35·Vdd V
Upper threshold voltage	0.65·Vdd V
Threshold voltage mismatch rejection ratio	33 dB (22 mV/V)
Peak DC current	1.9 uA

The PSRR is higher for the lower threshold (corresponding to rising edge at Schmitt trigger output) because the feedback PMOS transistor responsible for PSRR has a lower threshold voltage compared to the NMOS in the selected UMC 0.11um eFlash CMOS process. Therefore, the feedback PMOS is more saturated compared to the NMOS at low power supply voltage, resulting in superior PSRR. The minimum transistor width is 160 nm, but 270 nm was selected to reduce mismatch.

The implementation of time-setting RC-chain is not straightforward. Five options exist as listed in Table III.

TABLE III. CONSIDERED TIME-SETTING RC-CHAIN IMPLEMENTATIONS

RC Architecture	***Features***
MIM capacitor + internal metal resistor	Medium sensitivity (3000 ppm/K) Resistor nominal PV, large resistor area

RC Architecture	*Features*
MIM capacitor + poly-Si resistor	Low sensitivity (-1500 ppm/K) Uncertain TCR, resistor nominal PV
MIM capacitor + Si well resistor	Very high sensitivity (-8000 ppm/K) Uncertain TCR, resistor nominal PV, noise
MIM capacitor + external thermistor	High sensitivity (-4500 ppm/K) Good accuracy, higher power
External RC chain (with thermistor)	High cost, higher power, good accuracy

Evaluation of the various options of the RC-chain implementation clearly ruled out usage of an on-chip resistor for the time-constant setting. Conventional CMOS (metal) resistors have unstable nominal values, and other resistor types (poly-Si and well resistors) have unstable or poorly characterized temperature coefficients of resistance (TCR) as well. Therefore, for decent temperature sensor accuracy, an external, negative-temperature-coefficient (NTC) thermistor, fabricated in a dedicated semiconductor process, is necessary. An external, positive-temperature-coefficient (PTC) thermistor is possible as well, but not optimal because of lower sensitivity.

For the capacitor component of the RC-chain, the situation is reverse. MIM (metal-insulator-metal) capacitors available in the mixed-signal CMOS process have low, well-characterized temperature coefficients, and nominal capacitances defined with tolerances below 1%. This is comparable to even the best external NP0 ceramic or film (especially PPS film) capacitors. Therefore, the capacitor part of RC chain can be safely implemented inside the CMOS chip.

Giving consideration to all limitations discussed above, the selection of the TDC (time-to-digital converter) architecture for the ultra-low-power temperature sensor becomes straightforward. The developed architecture is shown in Fig. 1.

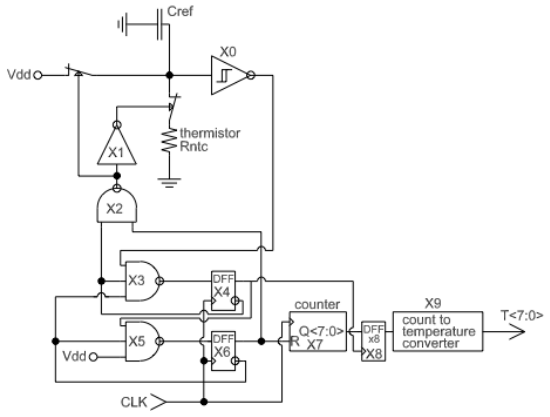

Figure 1. The simplified schematic of the developed temperature sensor.

The value of Cref was selected to be 300 pF and the nominal NTC thermistor, Rntc, was selected as 100 kΩ with TCR 3% gain tolerance. The thermistor was selected mostly for the sake of minimal thermistor package size (0.4 x 0.2 mm) in order to simplify the integration. The thermistor was integrated inside the package of the temperature sensor with direct chip-to-chip bonding wire interconnects.

B. Theory of Operation

The FDC converts a resistance, Rntc, at NTC input to an 8-bit 2's complement temperature code, XO<7:0>. A time reference made from a 2 MHz clock at the CLK input and reference on-chip capacitor, Cref, is used. Other clock frequencies can be used as well; up to 8 MHz if measurements at higher (>64 °C) temperatures are desired. The sensor requires a crystal-stabilized 2 MHz input clock to operate in the nominal temperature range. Conversion takes between 6 µs and 128 µs with lower latency for higher temperatures. The sensor was found to survive continuous exposure to 120 °C as well as to -20 °C. At temperatures above 64 °C the output saturates at 63.5 °C (0x7F output code), while temperatures below -6 °C produce essentially random output because counter X7 (see Fig. 1) overflows before the Schmitt trigger X0 toggles.

The conversion equation is follows:

$$XO<7:0>=2T_{ambient}+T_{offset} \qquad \text{(Eq. 1)}$$

The conversion using the circuit in Fig. 1 proceeds as follows:

Initially, the outputs of X4 and X6 are low. The sensing node, NTC, is slowly discharged through Rntc. After the voltage at Cref falls below Vdd/3, the output of X0 goes high and the output of X4 goes high at next clock rising edge. Thus, the X8 clock input has a rising edge and the output of X7 is stored in X8.

At the next clock cycle, the output of X6 becomes high, resetting the counter X7. Simultaneously, SW1 (connected to the power supply) is closed while SW2 (connected to Rntc) is opened, charging Cref node and forcing the output of X0 to "low".

On the next rising edge of the clock after the output of X0 switches to "low", the output of X4 will switch to "low" as well. At this point, the digital code latched by X8 appears on the output of X8. The X9 combinatorial block (28 low-leakage gates) converts the time measured by the counter to the temperature according to Eq. 1.

One clock cycle later, X6 switches to "low", discharging Csens, and the conversion cycle starts over.

III. TEMPERATURE SENSOR IMPLEMENTATION

Ten temperature sensor IC chips were manufactured in UMC 0.11um eFlash CMOS process, packaged in CERDIP-20 packages and integrated with the ERT-JZEV104H NTC thermistor on a breadboard. The photo of the chip is provided in Fig. 2.

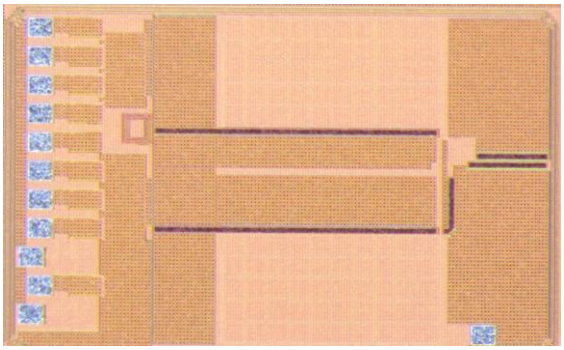

Figure 2. Developed temperature sensor before dicing.

The pad on the bottom-right of Fig. 2 is for the thermistor connection, while digital pads are arrayed on the left. The chip size is 0.98 mm x 1.62 mm including a 0.1 µm cut line for dicing. The pitch of digital pads is 80 µm.

40% of the chip area is taken by the 300 pF MIM reference capacitor, and most of remainder is high-density dummy patterns overlapping a 10 nF power supply bypass capacitor. Power supply bypass capacitor is implemented as a MOSFET capacitor utilizing the capacitance of the gate of the 3.3 V I/O transistors. Also, each of digital blocks (X9, X8 and others) are fitted with a separate power supply filter comprised of 45 Ω poly-Si resistors and 30 100 pF MOSFET capacitors. The pads were custom-designed to reduce the output slew rate to 10 V/µs. Also, special attention was paid at the layout level to avoid high amplitude current consumption spikes, especially at counter X7. Counter delays were tweaked to reduce amplitude of power supply noise injected to rest of the chip. Without using an external bypass capacitor, and in a laboratory environment, these strict measures to reduce internal sources of power supply noise and attenuate external power supply noise, along with the good intrinsic PSRR of Schmitt trigger, have resulted in an operational temperature sensor with limited quantization-noise.

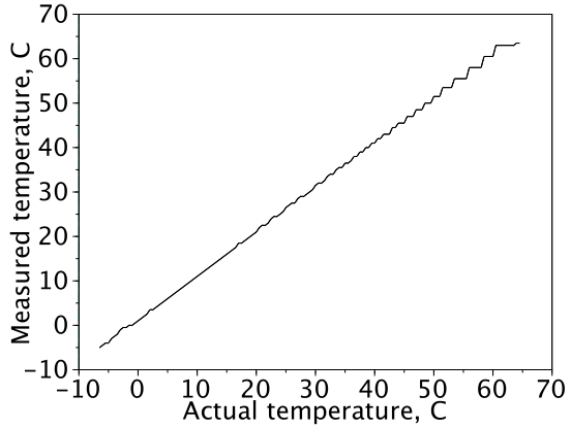

Figure 3. Measured transfer curve of the temperature sensor.

The transfer curve of temperature sensor was measured and the sensor was found to function adequately in the temperature range -6°C to 64°C, as illustrated in Fig. 3. The sensor was limited at lower temperatures by overflow of the time-to-digital converter, and limited at higher temperatures by increased quantization noise. The usable power supply range was found to be 0.75 V to 3.0 V, as illustrated in Fig. 4. At the lowest power supply voltage, the sensor become noticeably noisy (BER~10^{-4}), while higher power supply voltages resulted in a temperature offset due to self-heating.

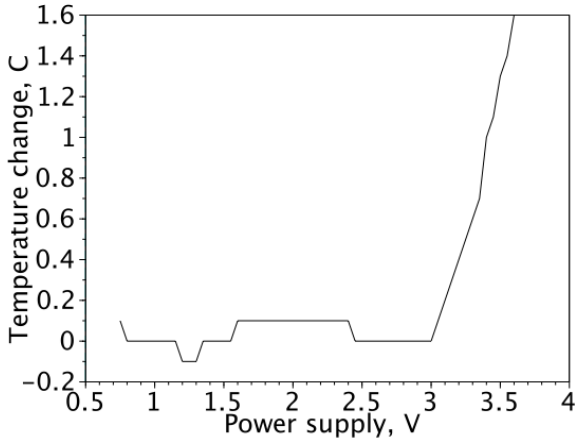

Figure 4. Power supply voltage to measured temperature sensitivity of the temperature sensor.

The power dissipation of the developed sensor was measured at 0 °C, with measurement results shown on Fig. 5. Accurate estimation of internal sensor power at other temperatures was not feasible because the power measurements included the current needed to drive the weak pull-down resistors on the digital output pads. Because of the circuit design, it was not possible to determine which portion of the power consumption was due to the pads and pull-down resistors, and which portion was due to the sensor itself. In future designs, a sensor without pull-down resistors at the digital outputs should be used to measure power dissipation as a function of temperature.

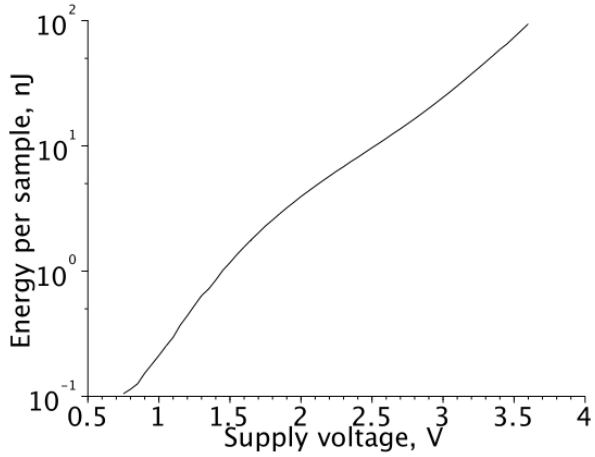

Figure 5. The measured energy dissipation of temperature sensor at 0 °C.

The stability and offset of the temperature sensor was studied on batch of 4 thermistors and 10 temperature sensors.

Although no read-out change was detected from of swapping thermistors, there was significant variation in read-out found between different temperature sensor chips. The gain error of the sensor was found to be $0.018 \pm 0.009\,{}^{o}C/_{o}C\,(1\sigma)$, consistent with the gain error of the external thermistor used in the design. The offset of the sensors at 0 °C was $1.4 \pm 0.5^{o}C(1\sigma)$. Finally, it was found that the developed temperature sensor have a maximum temperature measurement error of $2.5^{o}C(1\sigma)$ as designed and $0.9^{o}C(1\sigma)$ if batch-level 2-point calibration would be applied.

IV. Conclusion

A CMOS temperature sensor for the -6 °C to 64 °C temperature range with a simple 2's complement 8-bit parallel output with LSB equal to 0.5 °C was developed. Temperature sensor performance is summarized in the Table IV. The most attractive feature of the developed sensor is low power dissipation combined with fast measurement time: 1.1 µW at 0 °C while measurement takes 90 µs, resulting in the temperature sensor power figure-of-merit (FOM) 0.75 pJ/step (105 pJ/sample). This is the lowest value for any temperature sensor reported so far. The combination of low power and modest accuracy (error below 2.5 °C) makes the temperature sensor suitable for activity monitoring, agricultural and indoor environments monitoring, especially in energy-harvesting sensor nodes.

TABLE IV. The developed temperature sensor performance summary

Parameter	Value
Operating temperature range	-6 °C to 64 °C
Nominal gain	2LSB/°C
Input clock	2.00 MHz
Operating suppy voltage range	0.75 V to 3.0 V
RMS noise/repeatability	0.2 °C to 0.3 °C for T ≤ 0 °C, ~0 for T > 0°C
Conversion time, -6 °C	128 µs
Conversion time, 0 °C	90 µs
Conversion time, 20 °C	30 µs
Conversion time, 64 °C	6 µs
Power dissipation (0.75 V @ 0 °C)	1.1 µW
Maximum error, as-made	2.5 °C
Maximum error, batch-calibrated	0.9 °C

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